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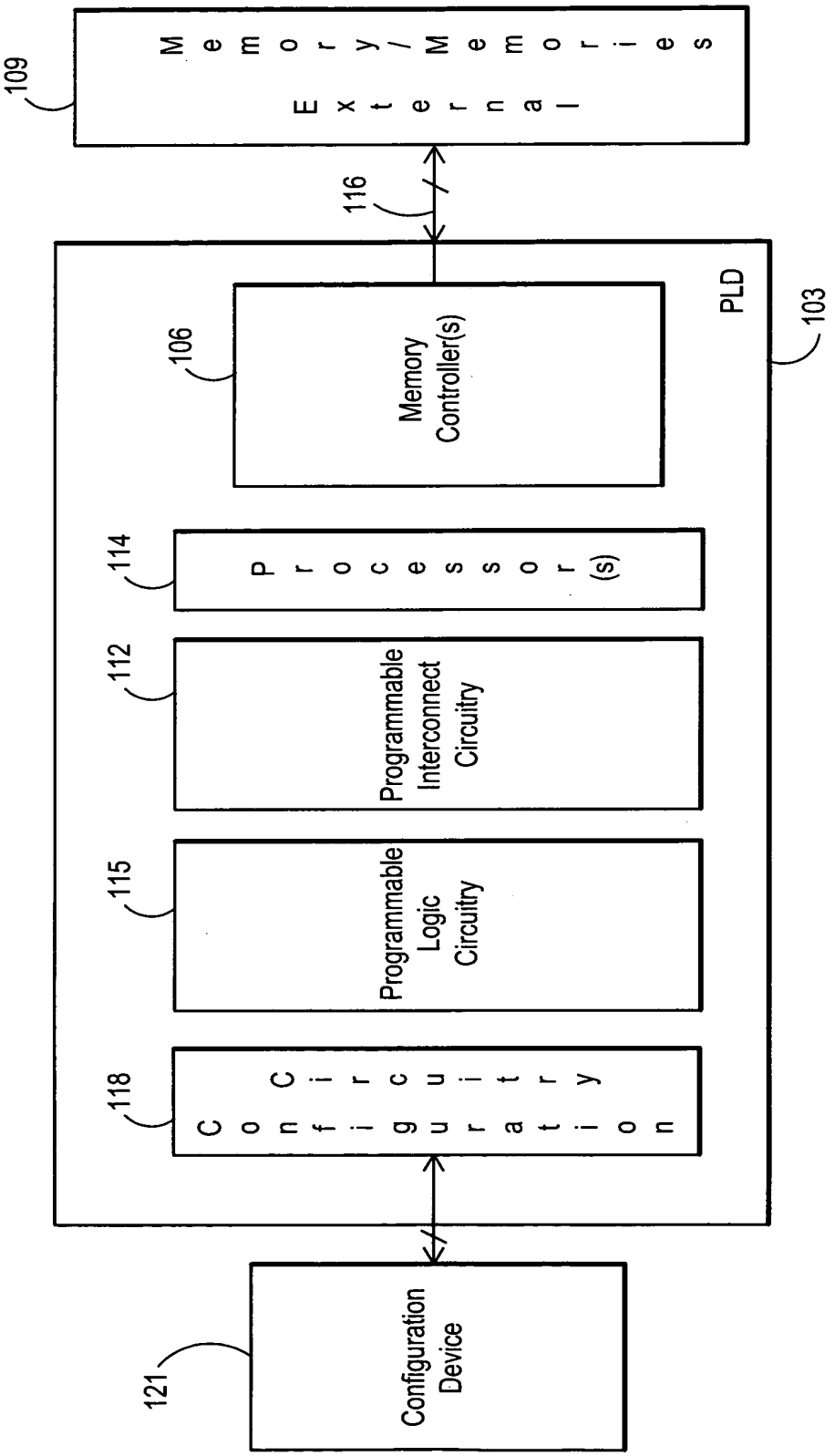

FIG. 1

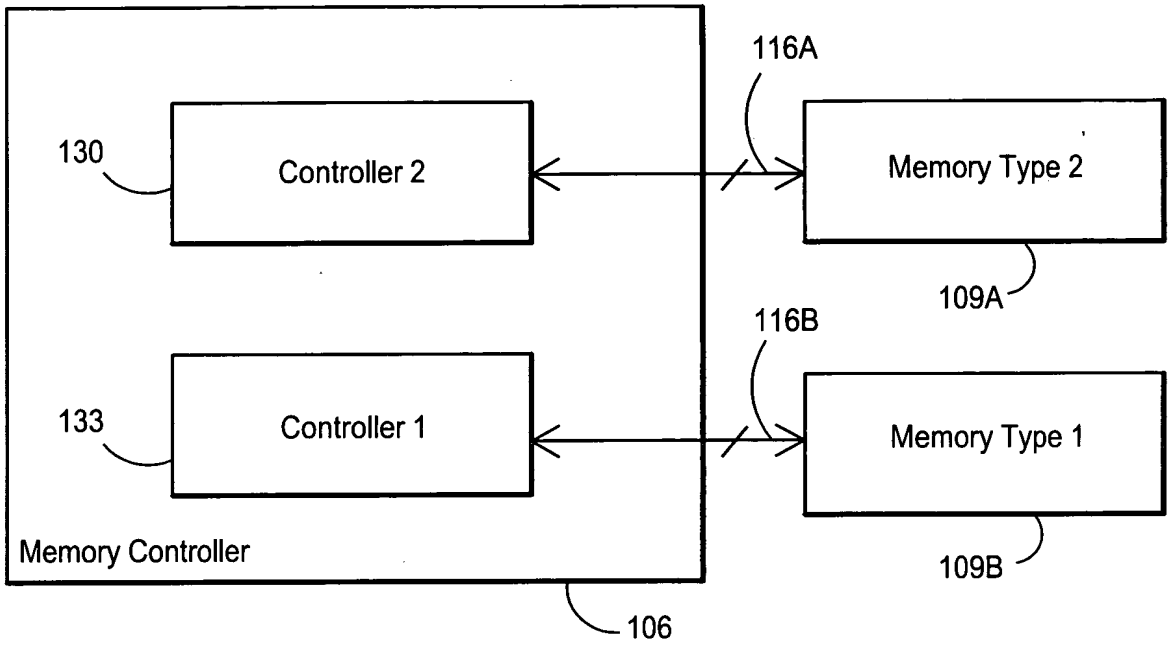
116A
130
Controller 2
Memory Type 2
109A
116B
133
Controller 1
Memory Type 1
109B
Memory Controller
106

FIG. 2

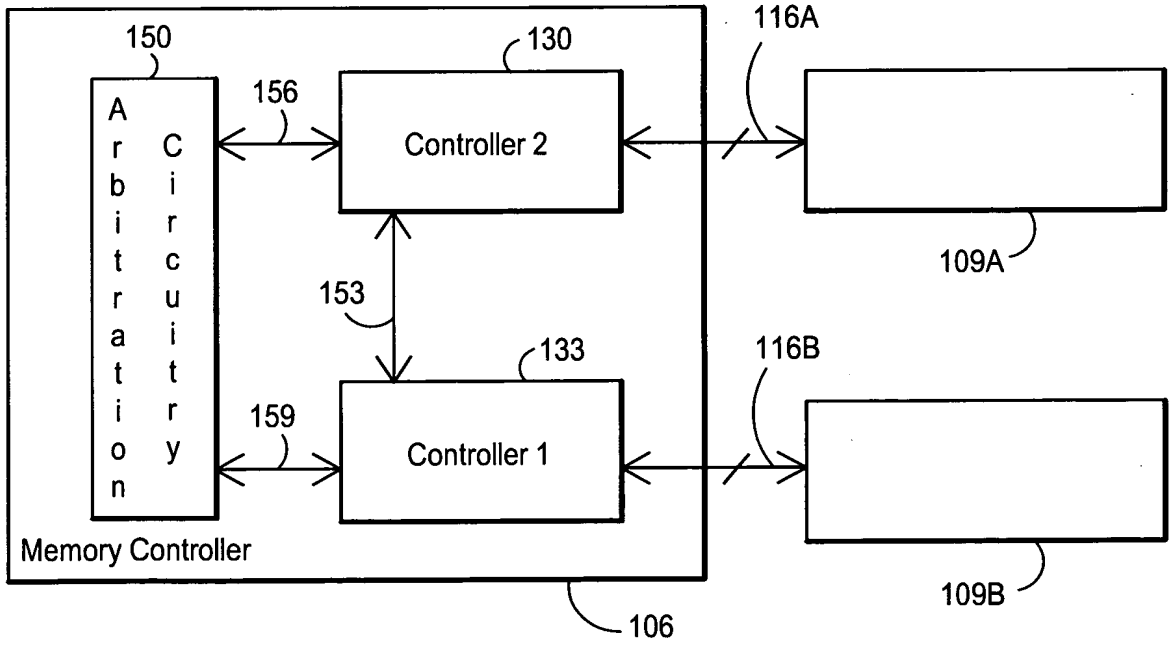
150
130
116A
156
Arbitration Circuitry
Controller 2
109A
153
133
116B
159
Controller 1
109B
Memory Controller
106

FIG. 3

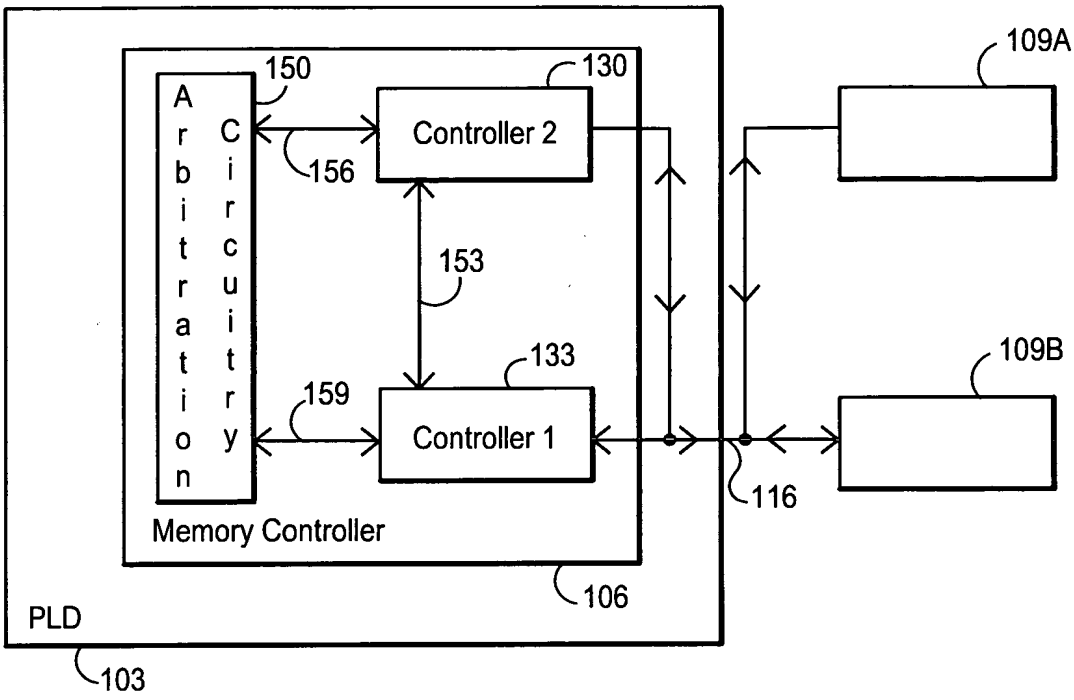
109A
150
130
Arbitration Circuitry
Controller 2
156
153
133
109B
159
Controller 1
116
Memory Controller
106
PLD
103

FIG. 4

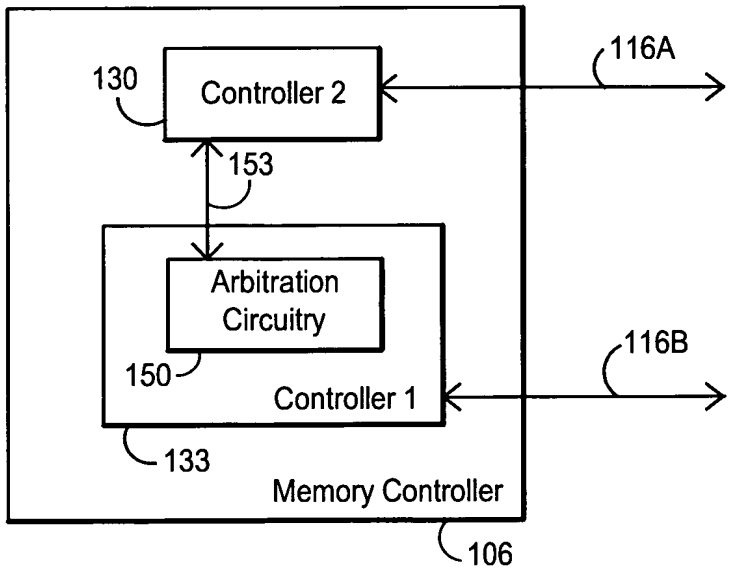
116A
130
Controller 2
153
Arbitration Circuitry
150
116B
Controller 1
133
Memory Controller
106

FIG. 5

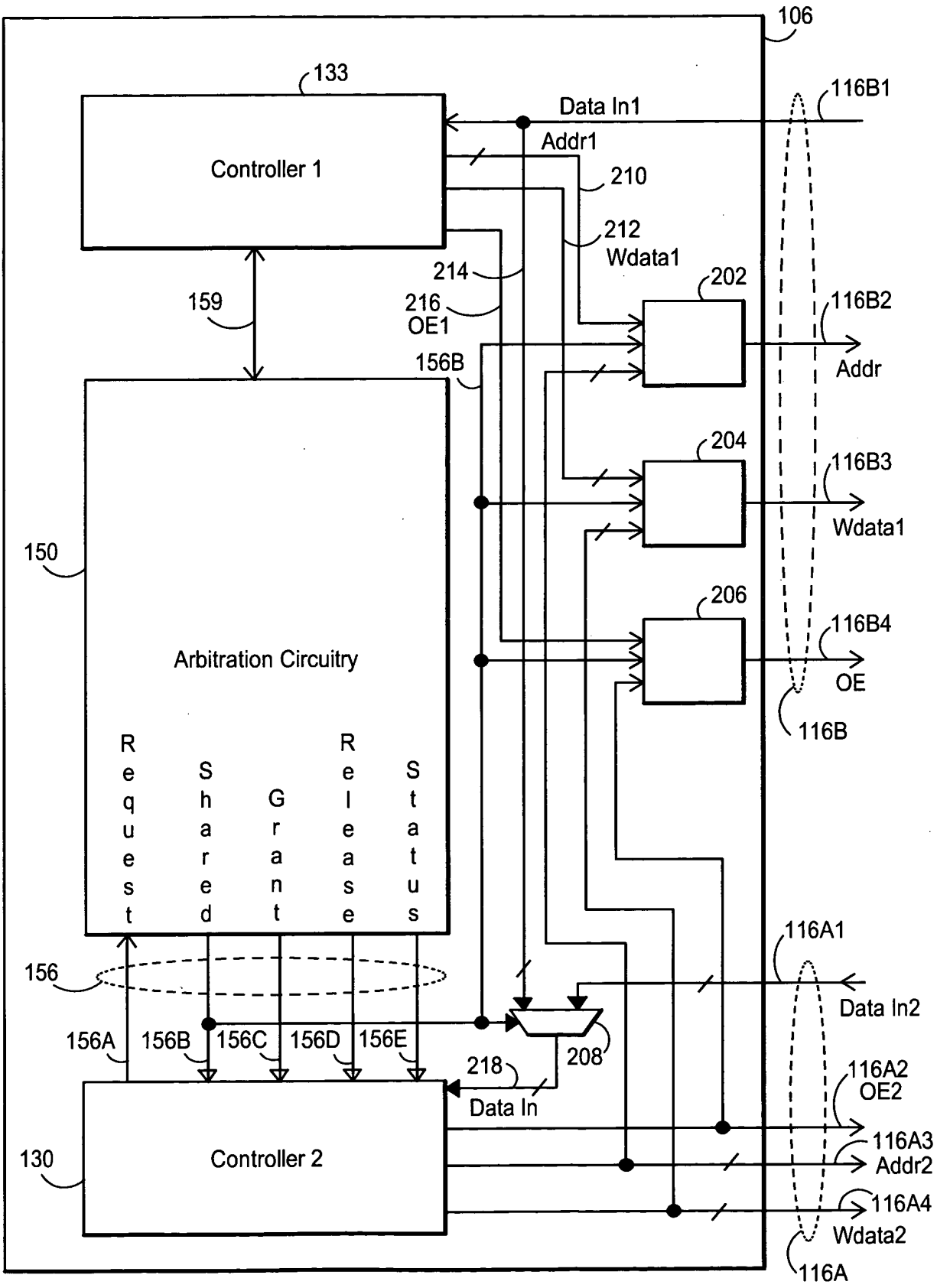
106
133
Controller 1
Data In1
Addr1
210
212
Wdata1
214
216
OE1
159
156B
202
204
206
116B1
116B2
Addr
116B3
Wdata1
116B4
OE
116B
150
Arbitration Circuitry
Request
Shared
Grant
Release
Status
156
156A
156B
156C
156D
156E
218
Data In
208
116A1
Data In2
116A2
OE2
116A3
Addr2
116A4
Wdata2
116A
130
Controller 2

FIG. 6

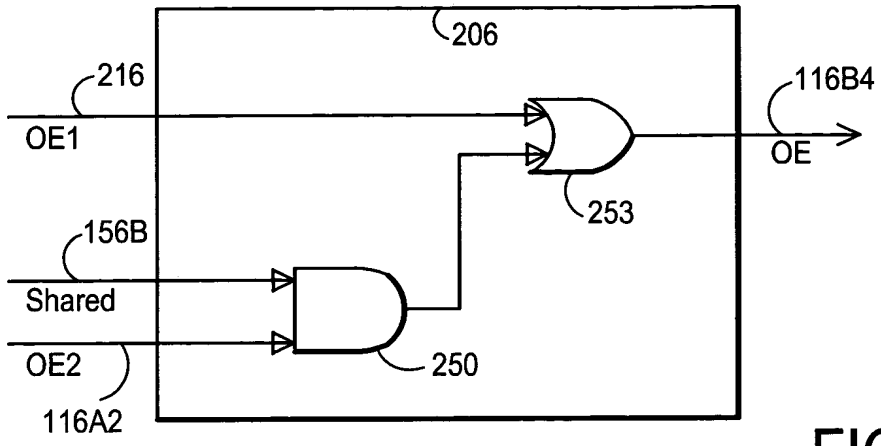
206
216
OE1
116B4
OE
253
156B
Shared
OE2
250
116A2

FIG. 7

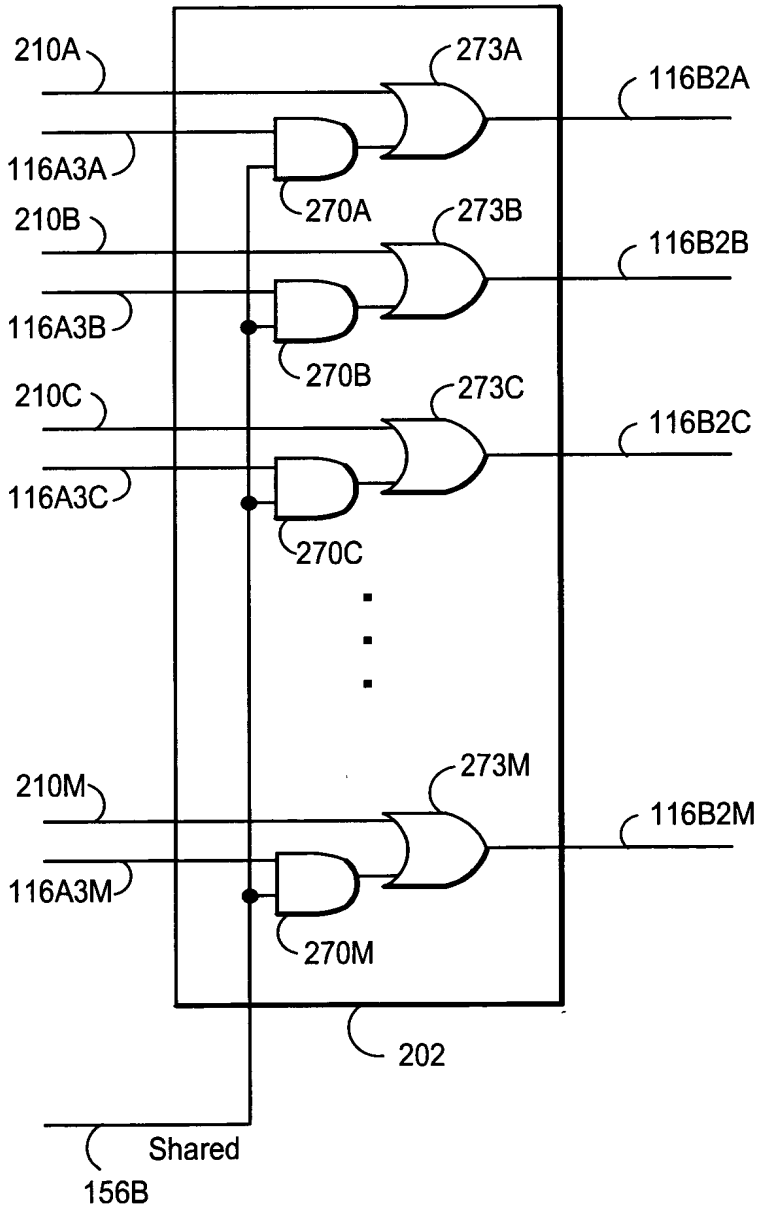
210A
273A
116B2A
116A3A
270A
210B
273B
116B2B
116A3B
270B
210C
273C
116B2C
116A3C
270C
210M
273M
116B2M
116A3M
270M
202
Shared
156B

FIG. 8

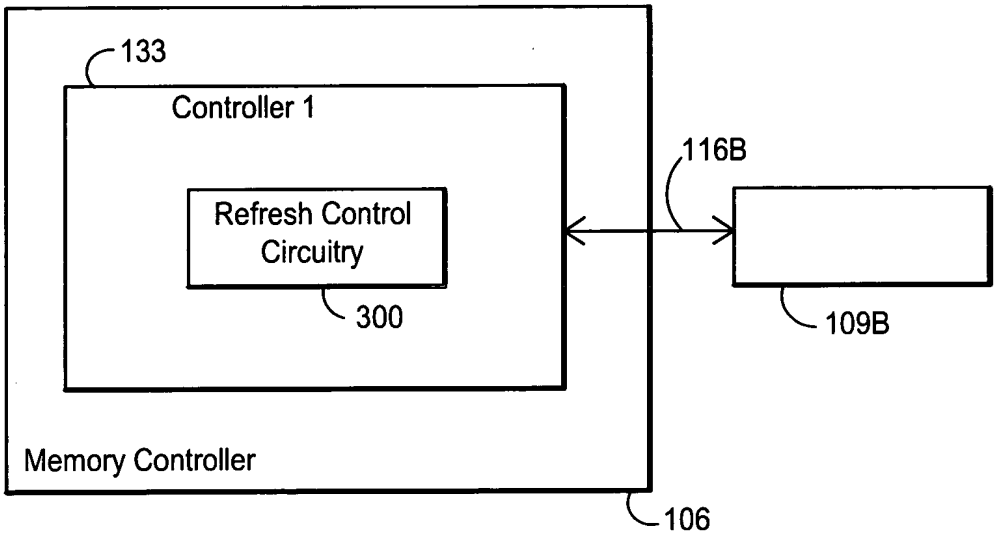
133
Controller 1
Refresh Control Circuitry
300
116B
109B
Memory Controller
106

FIG. 9

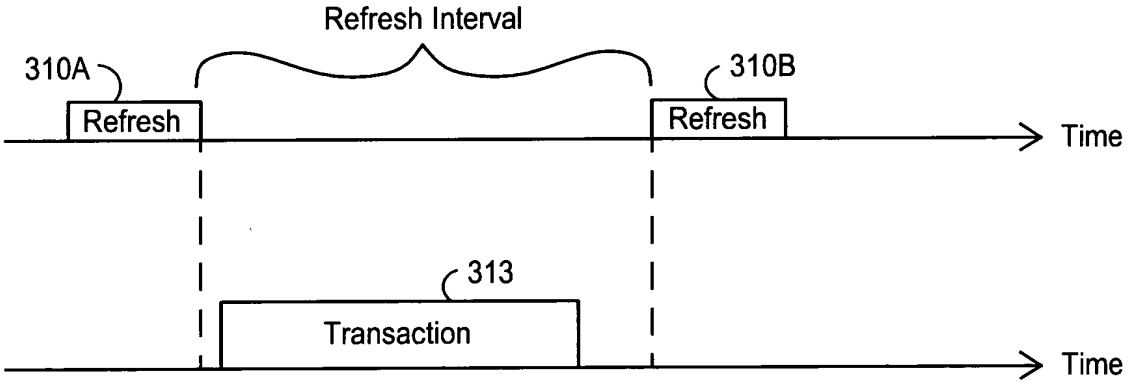
Refresh Interval
310A
Refresh
310B
Refresh
Time
313
Transaction
Time

FIG.10

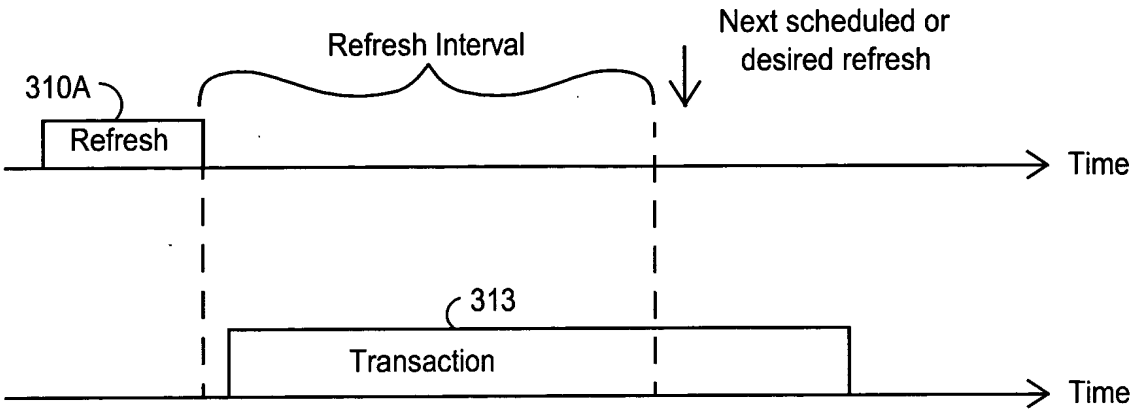
Refresh Interval
Next scheduled or
desired refresh
310A
Refresh
Time
313
Transaction
Time

FIG.11

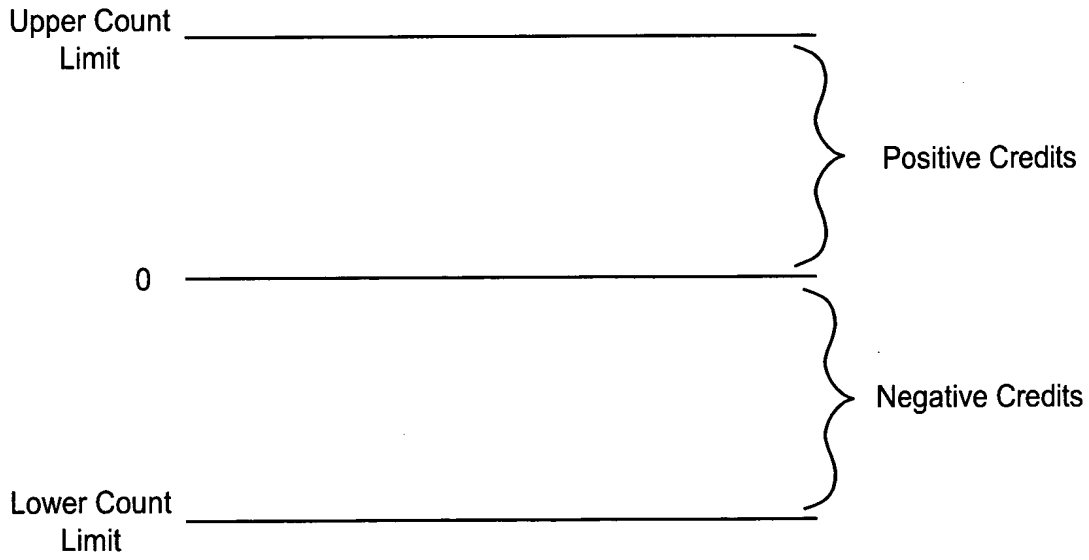
Upper Count
Limit
Positive Credits
0
Negative Credits
Lower Count
Limit

FIG.12